What is claimed is:

1. A semiconductor device comprising:

a plurality of bit-line pairs;

a plurality of word lines;

a plurality of memory cells provided at intersection points formed by the plurality of bit-line pairs and the plurality of word lines;

a plurality of sense amplifiers, each of which is provided for each given number of bit-line pairs from among the plurality of bit-line pairs;

a plurality of write amplifiers, each of which is provided for said each given number of bit-line pairs;

a control circuit that selectively connects one of the given number of bit-line pairs to the sense amplifier, and that selectively connects one of the given number of bit-line pairs to the write amplifier;

an error-correction circuit;

a data storing circuit for storing data to write; and

an address storing circuit for storing an address corresponding to the data to write;

wherein:

said error-correction circuit corrects an error of data read out corresponding to a first writing address, and then generates first data to write;

said data storing circuit stores the first data to write; and

after a second writing address is inputted into the address storing circuit, said write amplifier writes the first data to write to the memory cell.

2. A semiconductor device according to Claim 1, said semiconductor device further comprising:

a first data path for connecting between the sense amplifier and the error-correction circuit; and

a second data path for connecting between the write amplifier and the error-correction circuit.

3. A semiconductor device according to Claim 2, said semiconductor device further comprising a parity generation circuit,

wherein:

said second data path includes in its path the data storing circuit and the parity generation circuit.

4. A semiconductor device according to Claim 3, wherein:

said sense amplifier is a latching sense amplifier;

operation by which first read data from a memory cell corresponding to the first writing address is read out into the sense amplifier, and operation by which the parity generation circuit generates parity according to the first read data and then the parity is stored in the data storing circuit, are performed before the second writing address is

decoded; and

the second writing address is decoded, and subsequently second read data from a memory cell corresponding to the second writing address is stored in the sense amplifier, and after that, data stored in the data storing circuit is written to a memory cell corresponding to the first writing address.

5. A semiconductor device according to Claim 1, wherein:

said data storing circuit has the capacity large enough to store two pieces of data to write or more; and

said address storing circuit has the capacity large enough to store two addresses or more.

6. A semiconductor device according to Claim 5, said semiconductor device further comprising:

a comparator that compares an address stored in the address storing circuit with an address inputted into the semiconductor device to output the result of the address comparison.

7. A semiconductor device according to Claim 6, said semiconductor device further comprising a data input/output pad,

wherein:

said comparator compares some bits of the addresses; and

if the address inputted into the semiconductor

device is an address used for read operation, and if the addresses agree with each other, data stored in the data storing circuit is output to the data input/output pad, whereas if the addresses do not agree with each other, data of a memory cell corresponding to the address is read, and then the data is output to the data input/output pad via the error-correction circuit.

8. A semiconductor device according to Claim 1, wherein:

a size of a transistor forming the data storing circuit is larger than that of a transistor forming the memory cell.

9. A semiconductor device according to Claim 1, wherein:

said plurality of memory cells are SRAM memory cells.

10. A semiconductor storage device comprising:

a plurality of bit-line pairs extending in a first direction;

a first word line extending in a second direction that intersects the first direction;

a first plurality of memory cells including a transistor formed in a first semiconductor area of a first conductivity type, said first plurality of memory cells being provided at intersection points formed by the plurality of bit-line pairs and the first word line; and

a first plurality of areas for well tap that are the

first conductivity type, and that have impurity concentration higher than that of the first semiconductor area, said first plurality of areas for well tap being used to supply well potential to the first semiconductor area, wherein:

among the first plurality of memory cells, different addresses are assigned to the first memory cells that are put between two adjacent areas for well tap in the first plurality of areas for well tap.

11. A semiconductor storage device according to Claim 10, wherein:

said plurality of memory cells include a transistor formed in a second semiconductor area of a second conductivity type; and

said first semiconductor area and said second semiconductor area extend in a second direction, and are placed so that they are adjacent to each other.

12. A semiconductor storage device according to Claim 11, said semiconductor storage device further comprising:

a second plurality of areas for well tap that are the second conductivity type, and that have impurity concentration higher than that of the second semiconductor area, said second plurality of areas for well tap being used to supply well potential to the second semiconductor area;

wherein:

among the first plurality of memory cells, different addresses are assigned to the first memory cells that are put between two adjacent areas for well tap in the second plurality of areas for well tap.

13. A semiconductor storage device according to Claim 12, said semiconductor storage device further comprising:

a second word line extending in a second direction;

a second plurality of memory cells including a transistor formed in a third semiconductor area of the first conductivity type and a transistor formed in a fourth semiconductor area of the second conductivity type, said second plurality of memory cells being provided at intersection points formed by the plurality of bit-line pairs and the second word line;

a third plurality of areas for well tap that are the first conductivity type, and that have impurity concentration higher than that of the third semiconductor area, said third plurality of areas for well tap being used to supply well potential to the third semiconductor area; and

a fourth plurality of areas for well tap that are the second conductivity type, and that have impurity concentration higher than that of the fourth semiconductor area, said fourth plurality of areas for well tap being

used to supply well potential to the fourth semiconductor area;

wherein:

said third semiconductor area and said fourth semiconductor area extend in the second direction, and are placed so that they are adjacent to each other;

said second semiconductor area and said third semiconductor area are placed so that they are adjacent to each other;

said first plurality of areas for well tap are connected to said third plurality of areas for well tap by use of first plurality of well potential supply lines extending in the first direction;

said second plurality of areas for well tap are connected to said fourth plurality of areas for well tap by use of second plurality of well potential supply lines extending in the first direction; and

said first plurality of well potential supply lines and said second plurality of well potential supply lines are placed so that each of the first plurality of well potential supply lines and each of the second plurality of well potential supply lines are adjacent to each other.

14. A semiconductor storage device according to Claim 10, wherein:

said first conductivity type is P type;

said first memory cell includes first and second P-

channel type MISFETs, and third and fourth N-channel type MISFETs;

a drain of the third MISFET is connected to a gate of the fourth MISFET;

a drain of the fourth MISFET is connected to a gate of the third MISFET;

a source-drain path of the first MISFET is connected to one of the bit-line pair and a drain of the third MISFET;

a source-drain path of the second MISFET is connected to the other of the bit-line pair and a drain of the fourth MISFET;

gates of the first and second MISFETs are connected to the first word line; and

the first and second MISFETs are vertical MISFETs formed on the first semiconductor area.

15. A semiconductor storage device according to Claim 14, wherein:

said vertical MISFET includes a stacked vertical device into which a bottom part of device, a middle part of device, and an upper part of device are laminated, and a gate poly-silicon that is generated on a side wall of the stacked vertical device through gate oxide.

16. A semiconductor storage device comprising:

a plurality of bit-line pairs extending in a first direction;

a first word line extending in a second direction that intersects the first direction;

a first plurality of memory cells provided at intersection points formed by the plurality of bit-line pairs and the first word line;

a plurality of P well areas extending in the first direction; and

a plurality of N well areas extending in the first direction;

wherein:

each of the first plurality of memory cells includes first and second PMOS transistors, and first, second, third, and fourth NMOS transistors, said first and second PMOS transistors being formed in one of the plurality of N well areas, and said first, second, third, and fourth NMOS transistors being formed in a P well area that is in contact with both sides of the N well area in which the first and second PMOS transistors are formed; and

among the first plurality of memory cells, different addresses are assigned to first memory cells that are adjacent to each other in the second direction.

17. A semiconductor storage device according to Claim 16, said semiconductor storage device further comprising:

a plurality of P areas for well tap that are P type, and that have impurity concentration higher than that of

the P well areas, said plurality of P areas for well tap being used to supply well potential to the plurality of P well areas; and

a plurality of N areas for well tap that are N type, and that have impurity concentration higher than that of the N well areas, said plurality of N areas for well tap being used to supply well potential to the plurality of N well areas;

wherein:

a P well supply line for supplying power to the plurality of P areas for well tap and a N well tap supply line for supplying power to the plurality of N areas for well tap extend in the second direction.

18. A semiconductor storage device according to Claim 16, wherein:

the first memory cells which are adjacent to each other in the second direction share a sense amplifier.